The invention in which an exclusive right is claimed is defined by the following:

1. A method for simulating a stochastic discrete event system, comprising the steps of:

(a) providing a discrete event model for the stochastic discrete event system;

(b) specifying parameters describing how the stochastic discrete event system is to be simulated;

(c) as a function of the discrete event model and the parameters that are specified, creating a hardware description for the simulation in terms of a hardware description language;

(d) compiling the hardware description into a configuration file that is loaded into a hardware logic circuit to define a plurality of factor processing modules that are implemented by the hardware logic circuit, one factor processing module being provided for each factor that contributes to a rate of a discrete event process that occurs in the stochastic discrete event system;

(e) simulating the stochastic discrete event system with the hardware logic circuit, wherein the hardware logic circuit produces an intermediate simulated result for each factor using the factor processing module provided for the factor, and wherein for each stochastic discrete event process carried out in the stochastic discrete event system, further comprising the step of logically combining the intermediate simulated results for all of the plurality of factor processing modules used for said process together to simulate the stochastic discrete event process, producing simulated results for the stochastic discrete event system.

2. The method of Claim 1, further comprising the step of discretizing the stochastic discrete event system in time, so that discrete events can only happen at uniformly spaced discrete instants in time comprising intervals of a specific duration, Δt.

3. The method of Claim 2, further comprising the step of changing a duration of the intervals, Δt, while the stochastic discrete event system is being simulated.

4. The method of Claim 2, wherein the parameters that are specified include a rate function specifying a rate that determines a probability of each discrete event occurring in a time interval of a specific duration.

5. The method of Claim 4, further comprising the step of automatically dynamically optimizing the specific duration of time so that an approximation error no greater than a specified level is achieved in the simulated results.

6. The method of Claim 1, wherein the step of logically combining the intermediate simulated results comprises the step of logically ANDing the intermediate simulated results together.

7. The method of Claim 1, further comprising the step of enabling the user to edit the model for the stochastic discrete event system.

8. The method of Claim 7, further comprising the step of enabling the user to modify the parameters used, during the step of simulating the stochastic discrete event system.

9. The method of Claim 1, further comprising the step of presenting the simulated results to the user in at least one of a visual manner and an audible manner.

10. The method of Claim 1, further comprising the step of counting events in each processing module.

11. The method of Claim 1, further comprising the step of storing at least one of static rates and dynamic rates in connection with the factor contributing to the rate of the discrete event process associated with one of the plurality of processing modules, said at least one of the static rates and the dynamic rates being used to scale a net rate for the discrete event process.

12. The method of Claim 2, wherein each event process that is discrete comprises a chemical reaction.

13. The method of Claim 2, wherein each event process that is discrete comprises a chemical interaction.

14. A logic processor for simulating a stochastic discrete event process based upon a discrete event model and parameters that describe how the stochastic discrete event process is to be simulated, comprising:

(a) a communication port used to input the parameters and to control the simulation of the stochastic discrete event process;

(b) process supervisory module that monitors events; and

(c) a plurality of factor processing modules, each factor processing module including:

(i) at least one counter factor module;

(ii) at least one rate factor module; and

(iii) at least one discrete event process module, said at least one discrete event process module including a processing block for each factor that contributes to a rate of the stochastic discrete event process, said processing block producing an intermediate simulated result for the factor, intermediate simulated results for all processing blocks being logically combined by the discrete event process module to produce simulated results for the stochastic discrete event process.

15. The logic processor of Claim 14, wherein a stochastic discrete event system is simulated using the logic processor by combining a plurality of reaction process modules, each reaction process module comprising the factor processing modules of Claim 14(c).

16. The logic processor of Claim 14, wherein discrete events can only happen at uniformly spaced discrete instants in time comprising intervals of a specific duration, Δt.

17. The logic processor of Claim 16, wherein the intervals, Δt, can be varied while the stochastic discrete event process is being simulated.

18. The logic processor of Claim 16, wherein the parameters include a rate function that specifies a rate determining a probability of each discrete event occurring in an interval specific duration.

19. The logic processor of Claim 18, wherein the process supervisory module automatically dynamically optimizes the specific duration of time so that an approximation error no greater than a specified level is achieved in the simulated results.

20. The logic processor of Claim 14, wherein the discrete event process module includes an AND gate for logically ANDing the intermediate simulated results for all of the processing blocks together to simulate the stochastic discrete event process.

21. The logic processor of Claim 14, wherein the logic processor is coupled to a computer through one of the communication port and an interface bus, to enable at least one of:

(a) creation and editing of the discrete event model for use in creating a hardware definition language description of the discrete event model used by the logic processor;

(b) interactive user modification of parameters employed in simulating the stochastic discrete event process while said process is being simulated; and

(c) implementing a portion of the stochastic discrete event process with the computer.

22. The logic processor of Claim 14, wherein the simulation results are output through the communication port.

23. The logic processor of Claim 14, wherein each counter factor module includes:

(a) a register;

(b) a pseudorandom number generator that produces a pseudorandom number that is combined with a value stored in the register to produce a scaled value; and

(c) a comparator for comparing a counter value to the scaled value, producing the simulated result for the processor module.

24. The logic processor of Claim 23, wherein each counter factor module includes a bitwise AND logic element that mask specific bits in the pseudorandom number using the value stored in the register to produce the scaled value.

25. The logic processor of Claim 23, wherein the simulated result produced by each factor processing module comprises a pseudorandom bit stream at a rate that is proportional to one of the value stored in a register of the rate factor module and the counter value.

26. The logic processor of Claim 14, wherein each rate factor module includes:

(a) a register;

(b) a pseudorandom number generator that produces a pseudorandom number that is combined with a value stored in the register to produce a scaled value; and

(c) a comparator for comparing a rate value to the scaled value, for determining a rate used for scaling a net rate of the discrete event process.

27. The logic processor of Claim 26, wherein the rate value is provided by a rate factor module, said rate factor module storing or producing at least one of static rates and dynamic rates.

28. A method for simulating second-order and above event processes, comprising the steps of:

(a) discretizing the event processes in time, so that discrete events can only happen at substantially uniformly-spaced discrete instants in time, each of which occurs in a time increment selected so that the probability of the discrete event occurring during the time increment is much less than one;

(b) simulating a discrete event arrival process using a Bernoulli random process for each time increment;

(c) for each factor contributing to the event processes, determining a probability of an event relating to the factor occurring within the time increment; and

(d) determining a probability of the simulated second-order and above event processes by logically ANDing the probabilities of all of the factors contributing to the event processes.

29. The method of Claim 28, wherein the step of determining the probability of the simulated second-order and above event processes produces a result that is substantially equivalent to a product obtained by multiplying the probability for each factor contributing to the event processes.

30. The method of Claim 28, further comprising the step of dynamically optimizing the time increment to achieve an approximation error that is no greater than a defined value.

31. The method of Claim 28, wherein rates at which events occur are one of:

(a) time-varying functions;

(b) functions of the elapsed time since a last change in state;

(c) functions of a state of the simulation; and

(c) a constant.

32. The method of Claim 28, wherein the event processes are simulated in parallel.

33. The method of Claim 28, further comprising the step of creating a model of the event processes for use in the step of simulating the discrete event arrival process.

34. The method of Claim 33, further comprising the step of creating a hardware description corresponding to the model, said hardware description being used to automatically create a hardware logic circuit for simulating the discrete event arrival process.

35. The method of Claim 28, further comprising the step of enabling a user to input a plurality of parameters that control the step of simulating the discrete event arrival process.

36. The method of Claim 28, wherein each event process that is discrete comprises a chemical reaction.

37. The method of Claim 28, wherein each event process that is discrete comprises a chemical interaction.